

IN THE CLAIMS

Please modify the claims as set forth hereinafter:

1. (Currently Amended) A semiconductor device comprising:

a plurality of metal wire patterns which include a fine line pattern having a sub-micron width and pad patterns, said plurality of metal wire patterns being formed at a same pattern and being electrically connected to each other, an area of the fine line pattern being formed to be more than 1% of a total area of said plurality of metal wire patterns.

2. (Canceled)

3. (Previously Presented) The semiconductor device as recited in claim 1, wherein the pad patterns include connection pad patterns which electrically connect the pad patterns to the fine line pattern, said connection pad patterns being included in said total area.

4. (Previously Presented) The semiconductor device as recited in claim 1, wherein the plurality of metal wire patterns are made of aluminum or copper.

5. (Currently Amended) A semiconductor device comprising:

a plurality of metal wire patterns which include main fine line patterns having a sub-micron width, main pad patterns and dummy fine line patterns having a sub-micron width,

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said plurality of metal wire patterns being formed at a same pattern and an area of the dummy fine line patterns, which are connected to the pad patterns, being formed to be less than 1% of a total area of said plurality of metal wire patterns and also being less than a value obtained by dividing an area of the main fine line patterns by said total area.

6. (Original) The semiconductor device as recited in claim 5, wherein the dummy fine line patterns are formed parallel with the main fine line patterns at a distance of a width of the main fine line pattern.

7. (Previously Presented) The semiconductor device as recited in claim 5, wherein the plurality of metal wire patterns are made of aluminum or copper wire.

8. (Previously Presented) The semiconductor device as recited in claim 5, wherein the dummy fine line patterns do not form or contribute to any electric circuit.

9. (Canceled)

10. (Previously Presented) The semiconductor device as recited in claim 5, wherein the plurality of metal wire patterns further include dummy pad pool patterns, to which the dummy

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fine line patterns are connected, said dummy pad pool patterns and said dummy fine line patterns being electrically disconnected from the main fine line patterns and the main pad patterns.

11. (Currently Amended) The semiconductor device as recited in ~~claim 5~~, claim 14, wherein the plurality of metal wire patterns are made of aluminum or copper wire.

12. (Previously Presented) The semiconductor device as recited in claim 5, wherein the plurality of metal wire patterns further include connection pad patterns which electrically connect the main pad patterns to the fine line patterns, said connection pad patterns being included in said total area.

13. (Previously Presented) The semiconductor device as recited in claim 12, wherein the total area is represented by $A_p + A_c + A + d$, where, 'd' represents the area of the dummy fine line patterns, 'A_p' represents an area of the main pad patterns, 'A_c' represents an area of the connection pad patterns and 'A' represents the area of the main fine line patterns.

14. (New) A semiconductor device comprising:
a plurality of main metal wire patterns including main fine line patterns having a sub-micron width and main pad patterns which are electrically connected to each other;

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a plurality of dummy metal wire patterns including dummy fine line patterns having a sub-micron width and dummy pad patterns which are electrically connected to each other;

said plurality of main metal wire patterns and said plurality of dummy metal wire patterns being formed at a same pattern and being electrically disconnected from each other; and

an area of said dummy fine line patterns being formed to be less than 1% of a total area of said plurality of dummy metal wire patterns and also being less than a value obtained by dividing an area of the main fine line patterns by a total area of said plurality of main metal wire patterns.
